WHAT IS CLAIMED IS:

1. A method for detecting STI void of semiconductor wafer, comprising steps of

assigning a test region in a predetermined region of the wafer;

forming active areas, trenches between the active areas and gate lines intersecting with tthe active areas, said trenches being filled with dielectric, and said active areas having their adjacent portion reaching at least a predetermined length; and

measuring the electric values of said gate lines to determine whether there is a void formed in the trench.

2. The method as claimed in Claim 1, wherein said active areas in the testing region are formed as parallel strips.

3. The method as claimed in Claim 1, wherein odd ones of said gate lines are connected together, while even ones of the gate lines are connected together, so as to form a dual-comb structure.

4. The method as claimed in Claim 3, wherein said measuring step is to measure the potentials of the comb structure of the odd gate lines and the comb structure of the even gate lines.

5. The method as claimed in Claim 1, wherein the testing region is formed on a predetermined cutting line of the wafer.

6. A testing region structure for STI void detection of semiconductor wafer, said test region structure being formed on the wafer by a process synchronous with other portions of the wafer, said structure comprising:

a plurality of active areas, the adjacent portion between two active areas reaching at least a predetermined length;

a plurality of trenches formed between the active areas and being filled with dielectric; and

a plurality of gate lines intersecting with said active areas.

7. The structure as claimed in Claim 6, wherein said active areas in the testing region are

formed as parallel strips.

8. The structure as claimed in Claim 6, wherein the odd ones of the gate lines are connected together, while the even ones of the gate lines are connected together, so as to constitute a dual-comb structure.

9. The structure as claimed in Claim 6, wherein the testing region structure is formed on a predetermined cutting line of the wafer.